WHAT IS CLAIMED AND DESIRED TO BE SECURED BY LETTERS PATENT OF THE UNITED STATES IS:

5   1. A method of inserting buffers in a circuit design, comprising the steps of:

preparing a physical hierarchy of the circuit design with placed macros;

performing global routing on the physical hierarchy;

10   determining a number of buffers to be inserted on each edge of nets of the global routing for boosting timing performance of the nets;

calculating a position for each buffer; and

inserting a buffer configured to boost timing performance at 15 each calculated position.

2. The method according to Claim 1, wherein said buffers are inverters.

20   3. The method according to Claim 1, wherein said buffers are repeaters.

4. The method according to Claim 1, wherein said step of calculating intervals comprises the steps of:

identifying a set of at least one edge in said nets for inserting buffers; and

determining an optimal number of buffers to be inserted on each edge.

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    5.   The method according to Claim 4, wherein:

said step of determining an optimal number of buffers comprises the step of,

calculating, for each edge, the optimal number of buffers based on an optimal timing for the edge, a delay of the edge, and an impedance of the edge.

    6.   The method according to Claim 5, wherein:

said step of calculating the optimal number of buffers comprises calculating

$$C_x^{\,i} = T_{opt} - D^{i-1} - \frac{\left(R'_{eq} + \frac{1}{2}R'\right)C'}{(R_{eq}{}' + R')f'}$$

    ;

where $C_x^{\,i}$ is a capacitance contribution of a branch segment seen by a driving node of the branch;

T_{opt} is the delay of an optimal stage;

D is delay of the edge;

R_{eq}^i is an equivalent resistance of merged segments of a corresponding branch segment;

f^i is fanout of a corresponding branch segment;

R is a resistance of the edge; and.

5   C is a capacitance of the edge.

7.   The method according to Claim 5, wherein:

said step of calculating the optimal number of buffers includes the steps of:

10   determining a uniform load distribution for all connected branches; and

adjusting for a delay introduced by the inserted buffers.

8.   The method according to Claim 7, wherein:

15   said step of determining a uniform load distribution comprises calculating

$$D^i = R^i \left[\frac{C^i}{2} + (f_i - 1)C_x^{'} \right] + R^i_{eq}[C^i + (f_i - 1)C_x^{'}];$$

where:

D^i is the delay of the stage;

R^i is resistance of the branch;

20   R_{eq}^i is an equivalent resistance of merged segments of the branch;

Ci is capacitance of the branch; and

Fi is a fanout of the branch.

9. The method according to Claim 1, further comprising the steps of:

5   uniformly distributing a capacitance of each branch of the nets at a corresponding branch point;

determining a load at each branch point; and

checking if a buffer inserted at each branch point is capable of handling the loaded determined for that branch point.

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10. The method according to Claim 9, wherein said steps of determining a number of buffers and calculating a position of each buffer comprises:

identifying a driver of a net to have buffers inserted;

15   performing a breadth first search (BFS) of the net starting at the identified net driver and processing all connected edges;

performing a depth first search (DFS) starting at a next stage in the net; and

for each edge, determining a number of buffers to be inserted

20   on each edge of nets of the global routing for boosting timing performance of the nets, and calculating a position for each buffer.

11. The method according to Claim 10, further comprising the steps of:

determining an actual capacitance of wires added to a branch at a branch point in a net;

5   using the actual capacitance in determining the number and position of buffers; and

redistributing capacitance comprising a difference between a calculated branch capacitance and the actual capacitance to other segments at said branch point.

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12. The method according to Claim 10, further comprising the steps of:

summing of resistances in all segments between a driver to a current segment being processed;

15 determining a sum of delays caused by the summed resistances; and

passing the summed resistances and delays on to a next segment to be processed.

20 13. The method according to Claim 1, wherein:

said method is embodied in a set of computer instructions stored on a computer readable media;

said computer instructions, when loaded into a computer, cause the computer to perform the steps of said method.

14.   The method according to Claim 13, wherein said computer instruction are compiled computer instructions stored as an executable program on said computer readable media.

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15.   The method according to Claim 1, wherein said method is embodied in a set of computer readable instructions stored in an electronic signal.

10   16.   The method according to Claim 1, further comprising the steps of:

identifying a set of staircase edges in the circuit design;

forming a merged segment of all segments in the staircase at a preselected layer;

15   scaling a length of each staircase segment by a ratio taking into account parameters of the staircase and the merged layer;

determining if any of the segments can be sped up using an inserted buffer; and

20   inserting buffers on the merged edge if the segment can be sped up.

17.   The method according to Claim 16, wherein said ratio comprises a ratio of a segment per unit length resistance and a per unit length resistance of the merged layer.

18.   The method according to Claim 16, wherein said step of determining if any of the segments can be sped up comprises, determining if the ratio of a pure wire delay of the merged segment to that of an isolated buffer delay is greater than or less than 1.

19.   The method according to Claim 16, wherein said step of inserting buffers comprises inserting buffers at a distance of l_{crit} from one of a start of the merged segment and a preceeding buffer.

20.   A method of correcting polarity with a minimized number of inverters in at least one path within a network, comprising the steps of:

marking all branch nodes with a polarity of a signal emanating from a driver up to the branch node being marked;

marking all sinks with a polarity of a signal emanating from a driver up to the branch node being marked;

traversing the network from each sink to an immediate branch node;

calculating a cost of correcting polarity of each sink;

carrying backwards the calculated cost to each sink; and

repeating said steps of traversing, calculating, and carrying

until a root of the network is reached; and

5   forward visiting the network and inserting inverters to fix

the polarity.

21.   The method according to Claim 20, wherein said step of

calculating a cost comprises:

10   determining a minimum cost between each of,

fixing the polarity on the segment driving the branch node,

and

fixing the polarity on branches stemming out of the branch

node; and

15   if downstream nodes of the branch node have a correct

polarity, then storing zero at the branch node and carried

backwards to an upstream branch node.

22.   The method according to Claim 20, further comprising the

20 step of:

storing a directive to indicate whether the minimum cost is

associated with inserting an inverter on a trunk feeding the

branch point or whether the inverter(s) are inserted on downstream

segment(s).

23.   The method according to Claim 20, wherein said cost is 1 or 0 depending on whether polarity is even or odd.

5   24.   The method according to Claim 20, wherein:

said method is embodied in a set of computer instructions stored on a computer readable media;

said computer instructions, when loaded into a computer, cause the computer to perform the steps of said method.

10   25.   The method according to Claim 24, wherein said computer instruction are compiled computer instructions stored as an executable program on said computer readable media.

15   26.   The method according to Claim 20, wherein said method is embodied in a set of computer readable instructions stored in an electronic signal.